

FIG. 1A

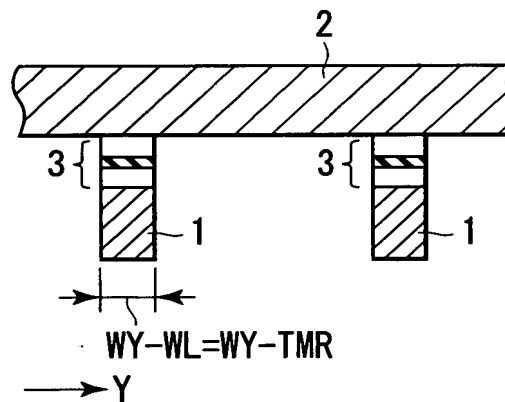


FIG. 1B

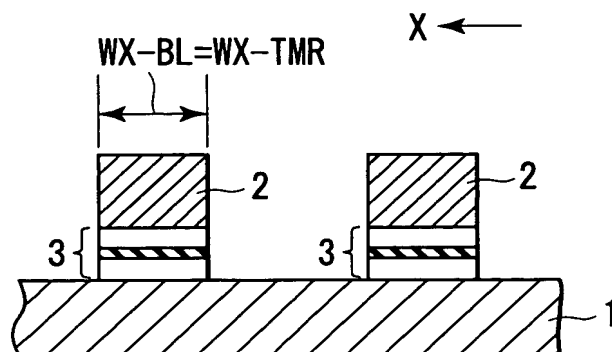


FIG. 1C

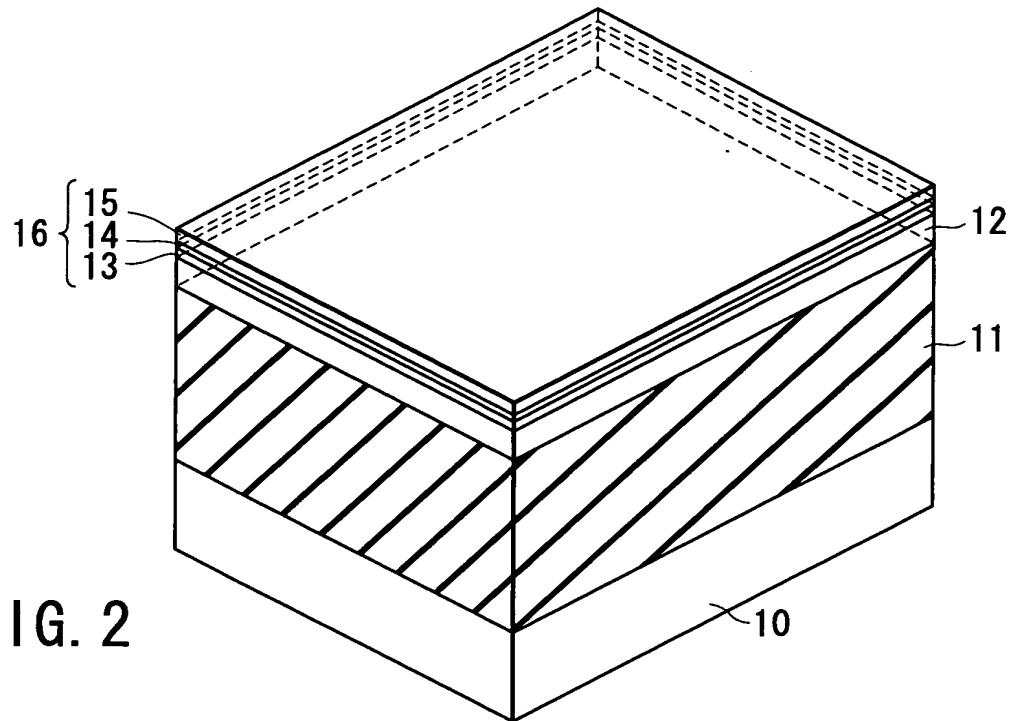


FIG. 2

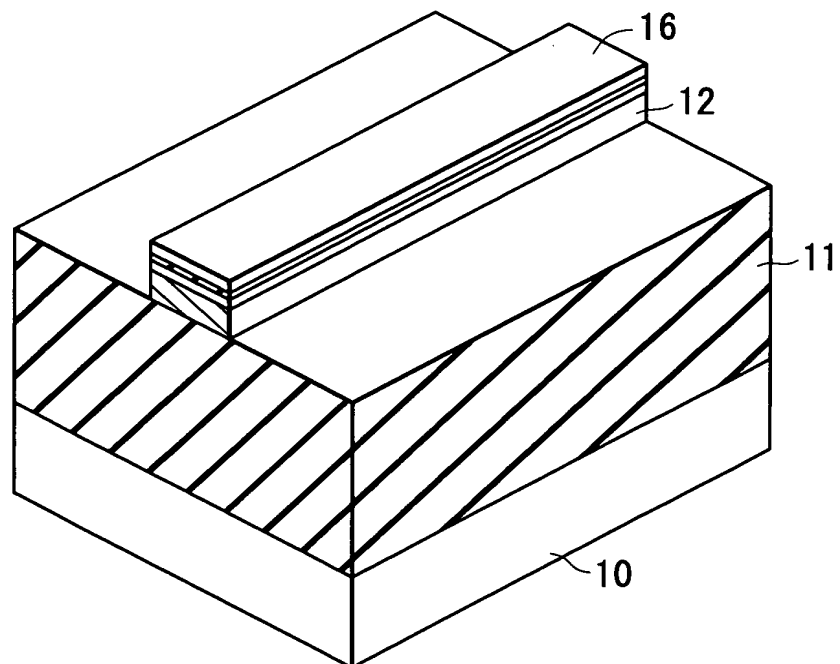


FIG. 3

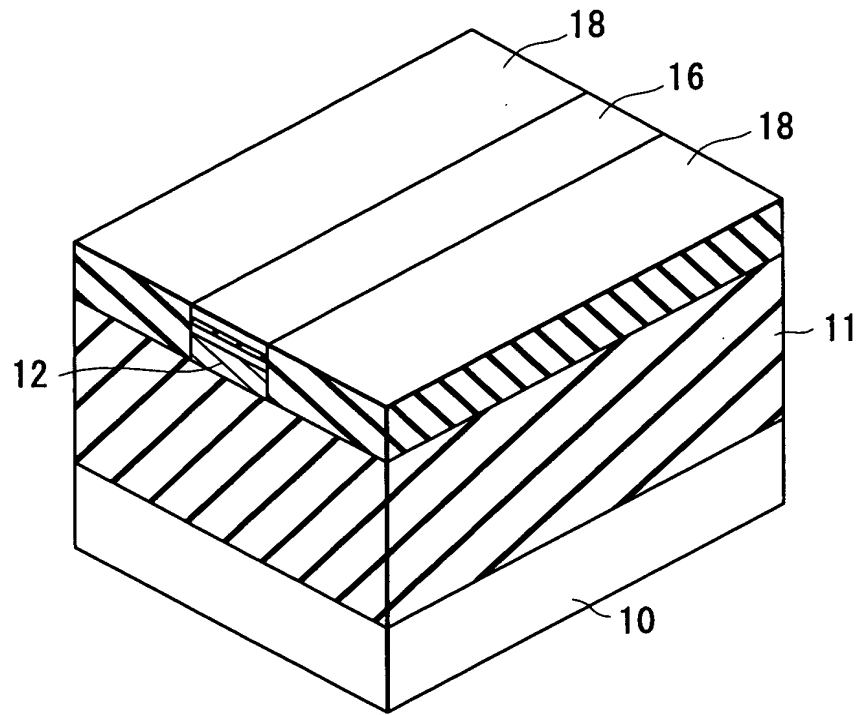


FIG. 4

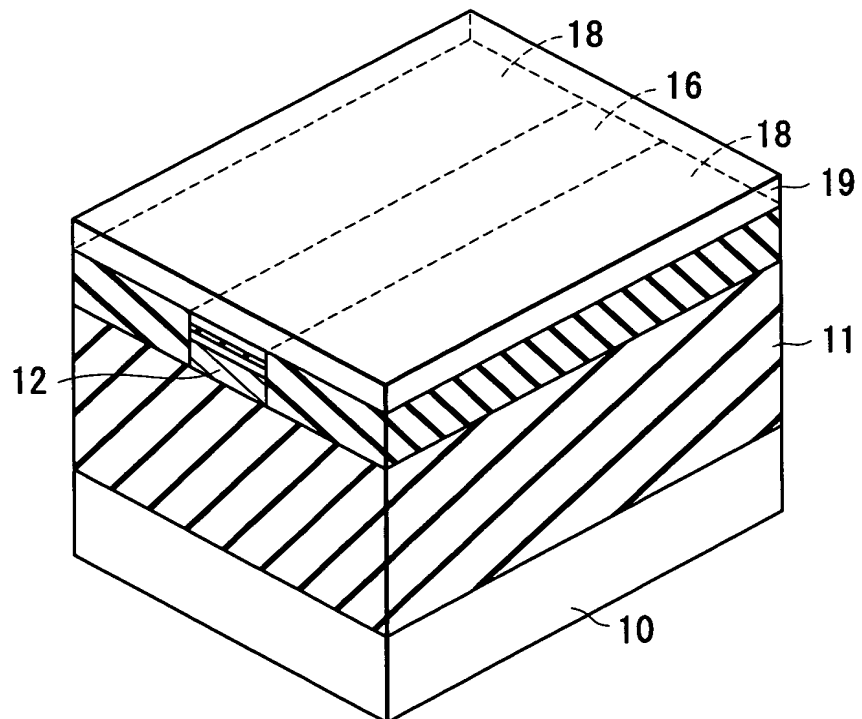


FIG. 5

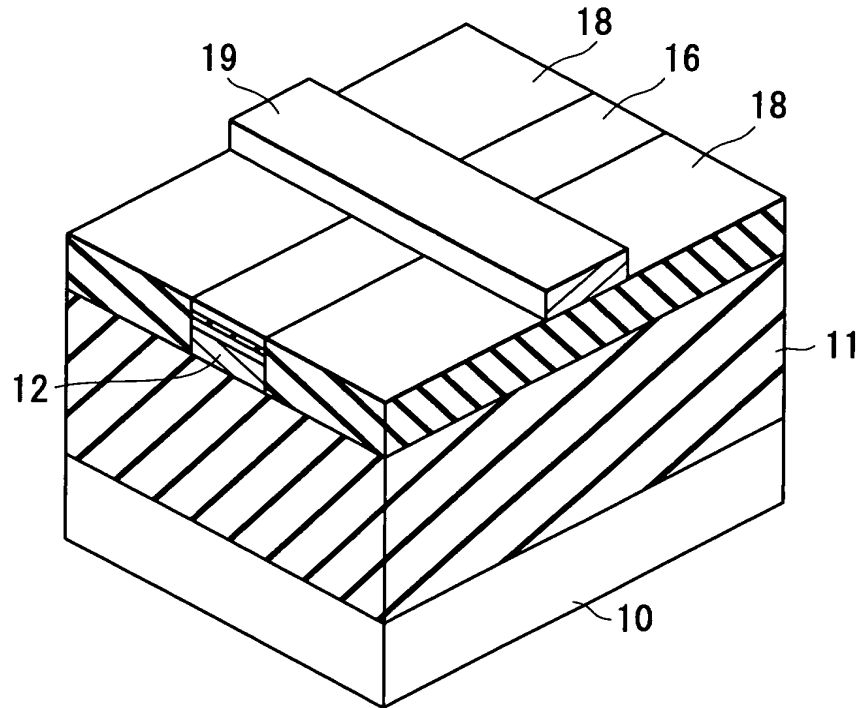


FIG. 6

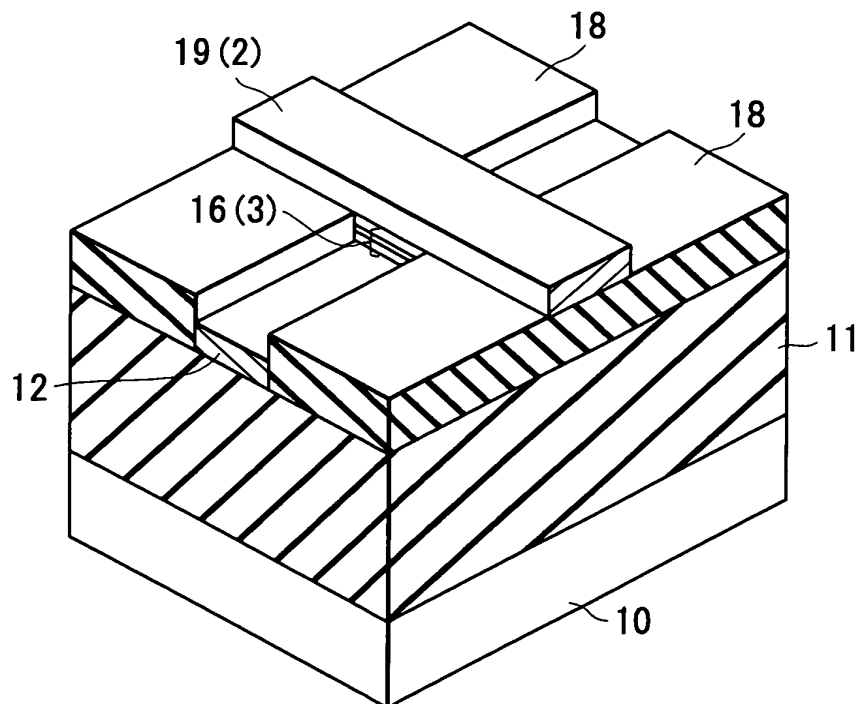
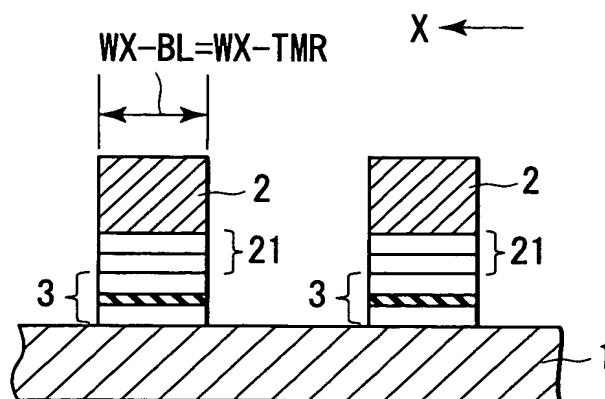
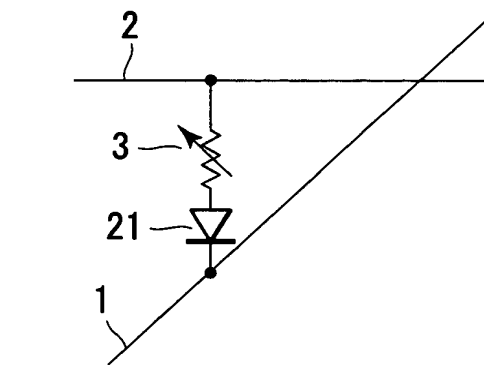
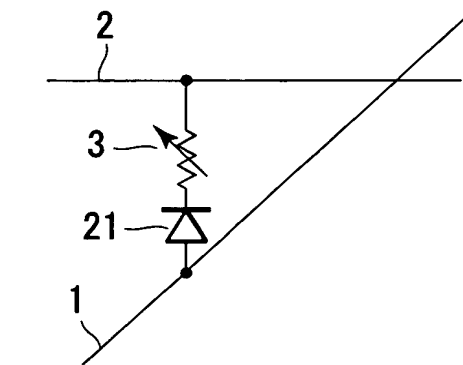
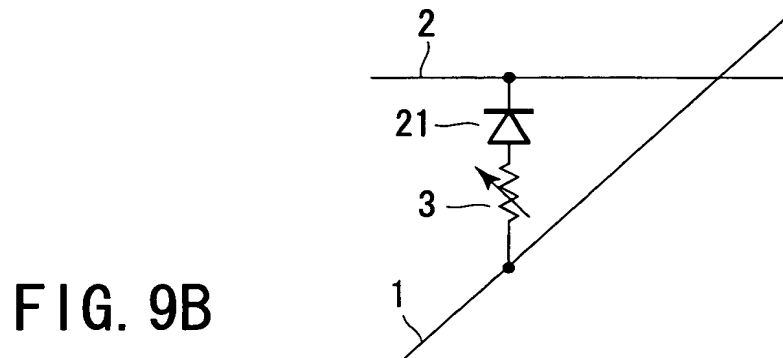
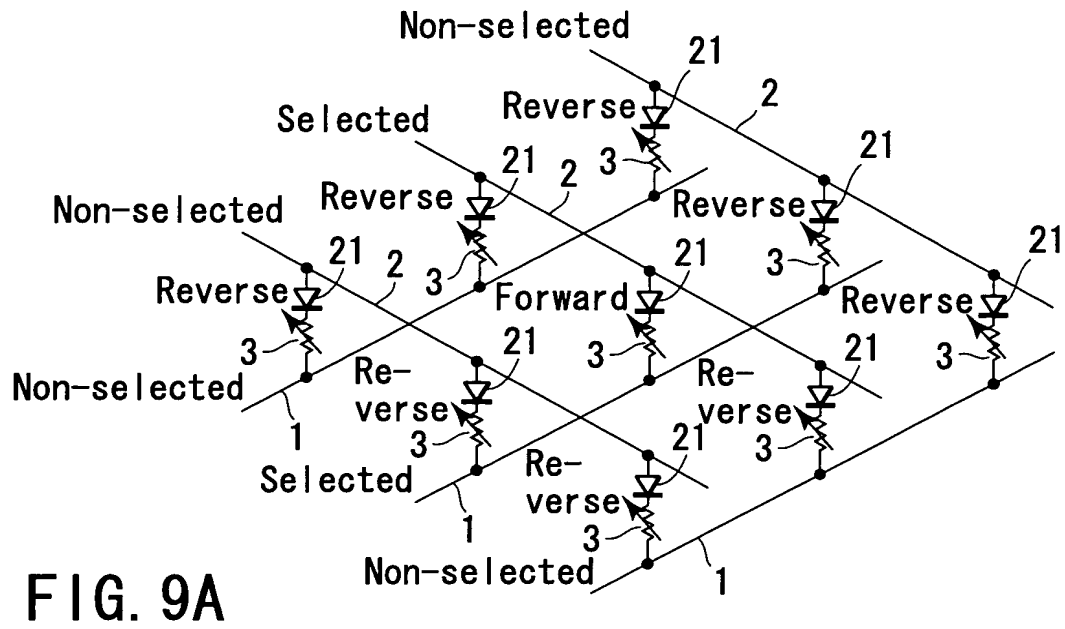
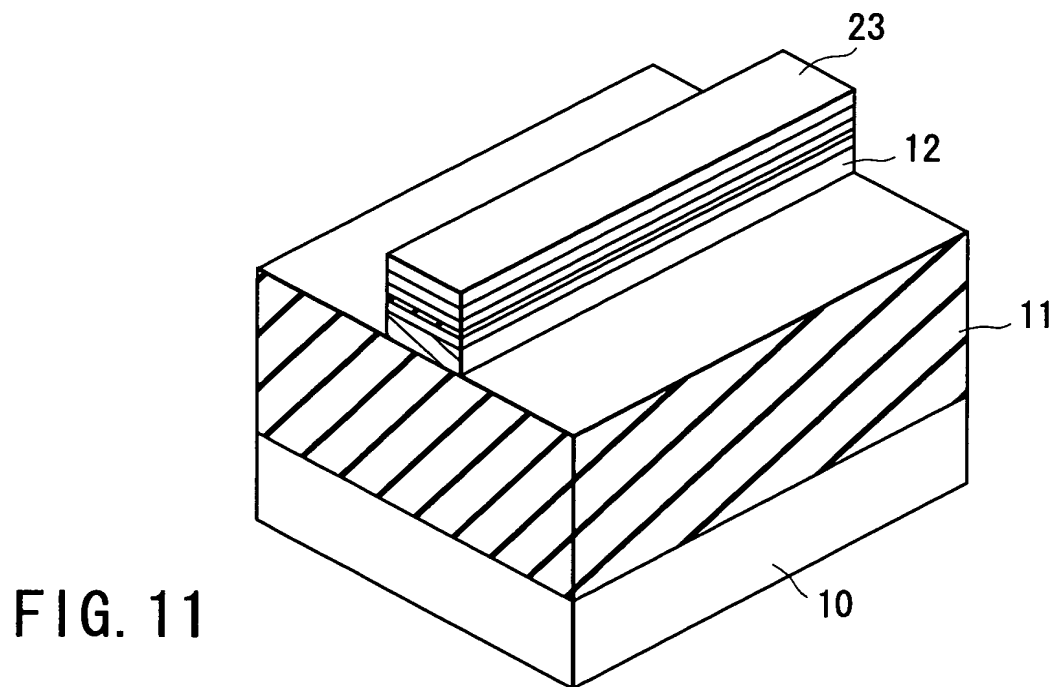
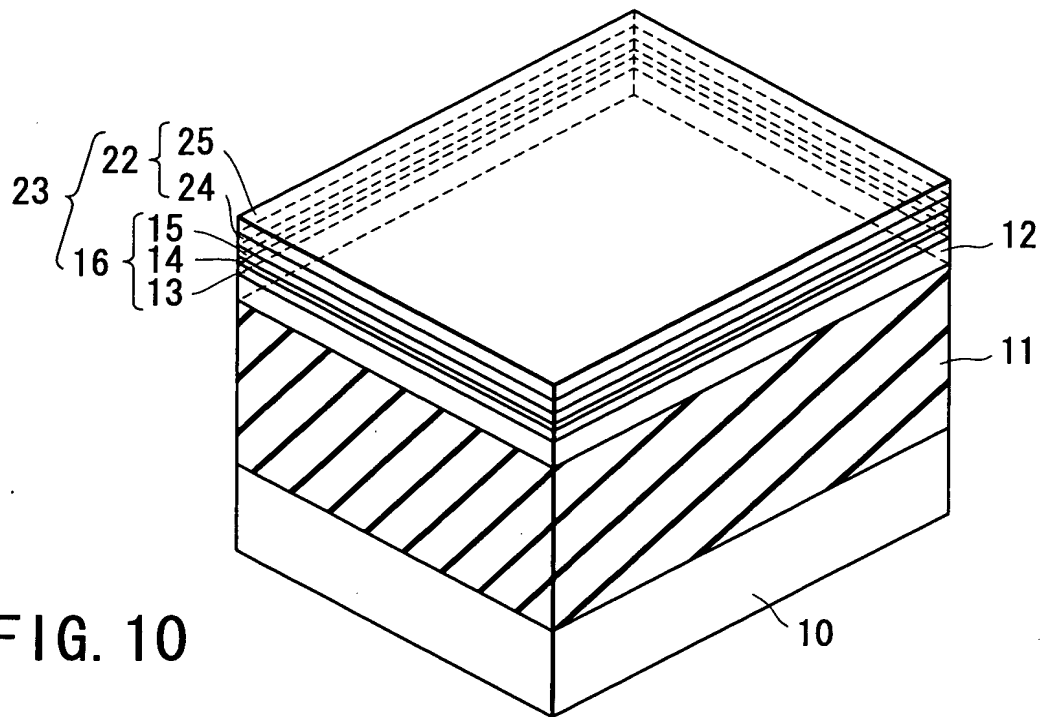


FIG. 7







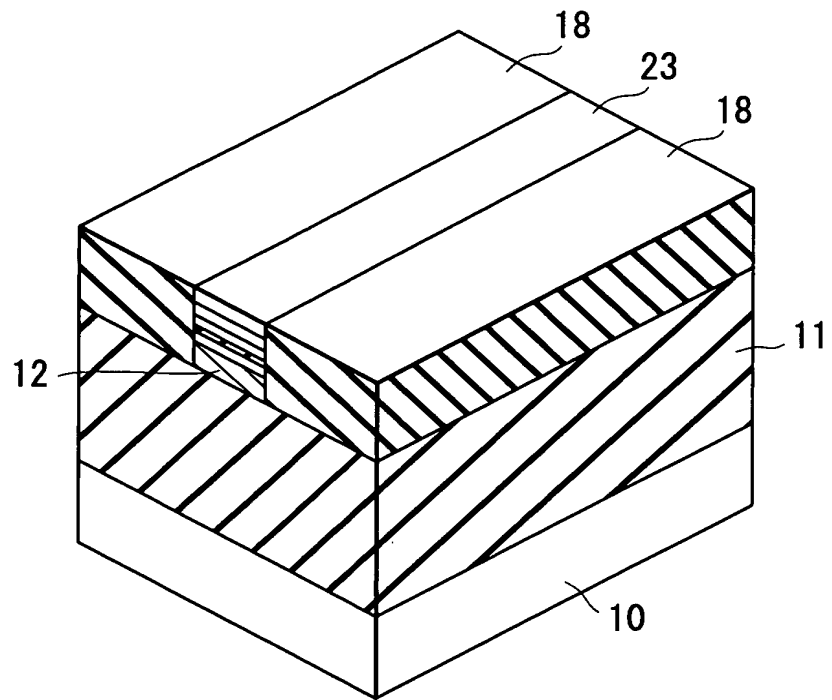


FIG. 12

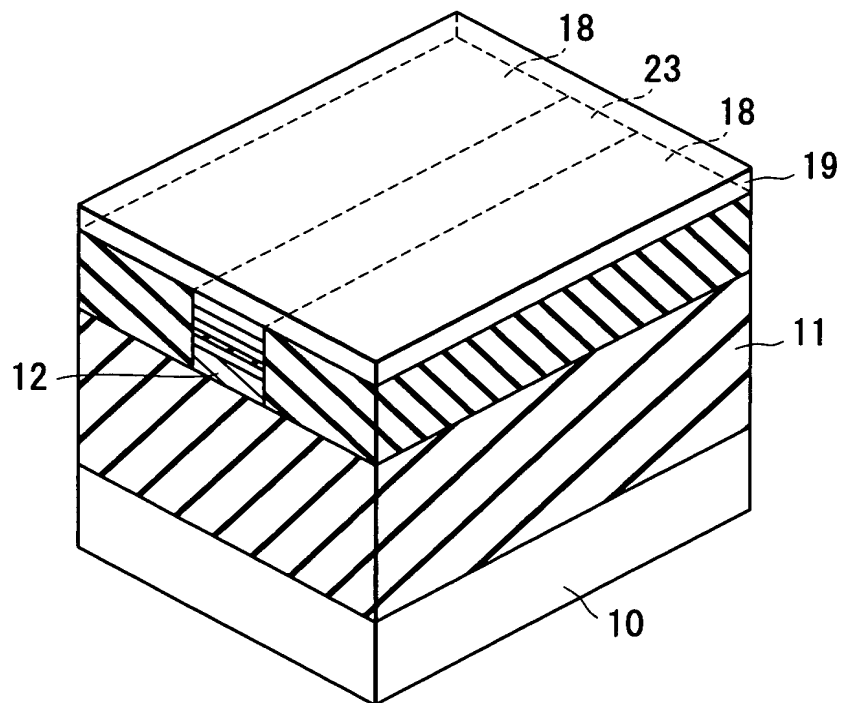


FIG. 13



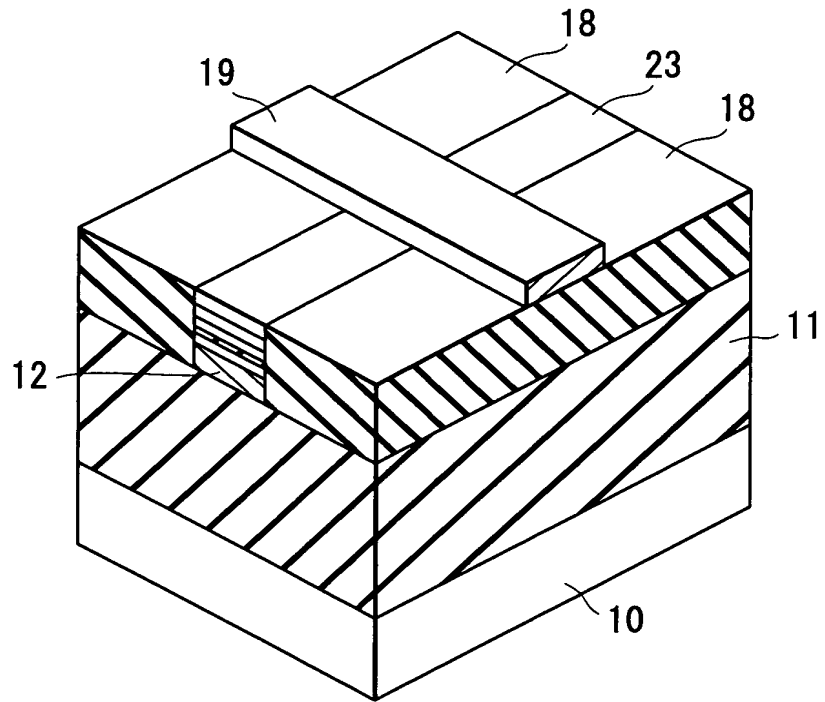


FIG. 14

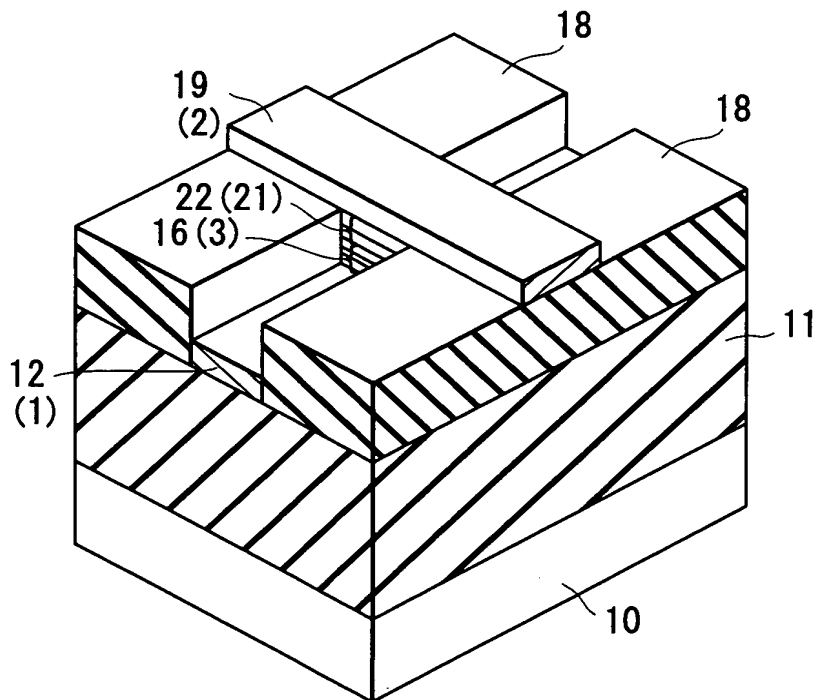


FIG. 15

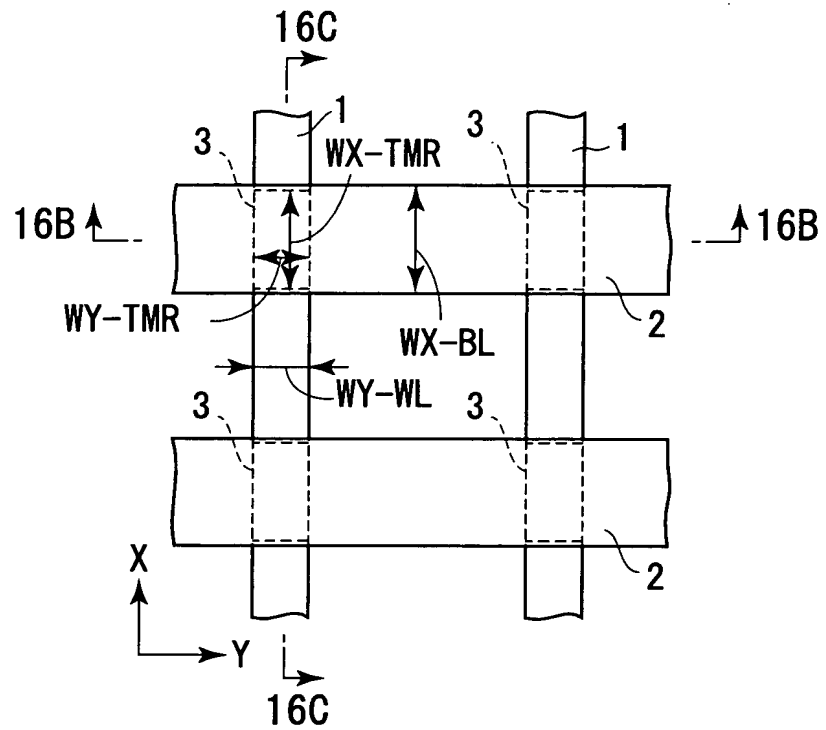


FIG. 16A

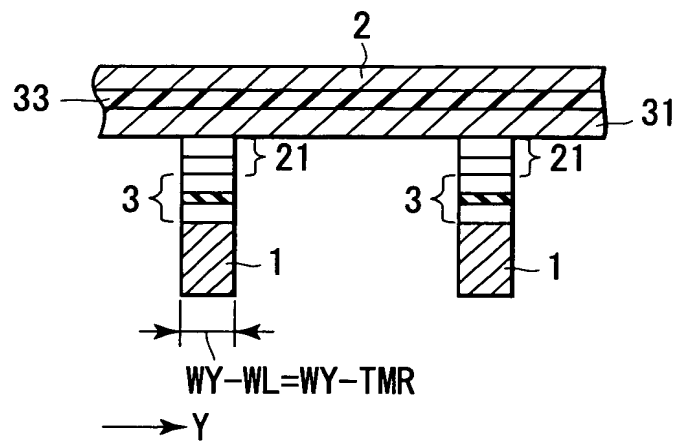


FIG. 16B

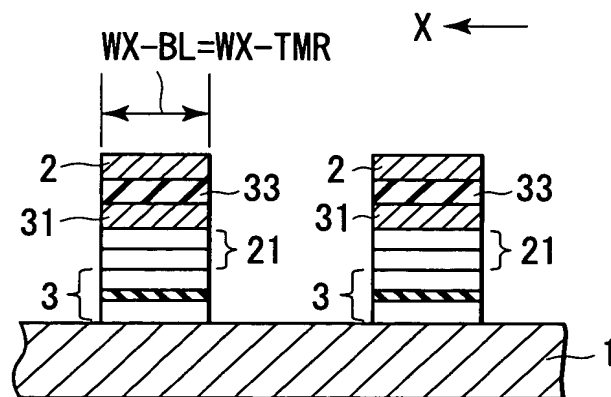


FIG. 16C

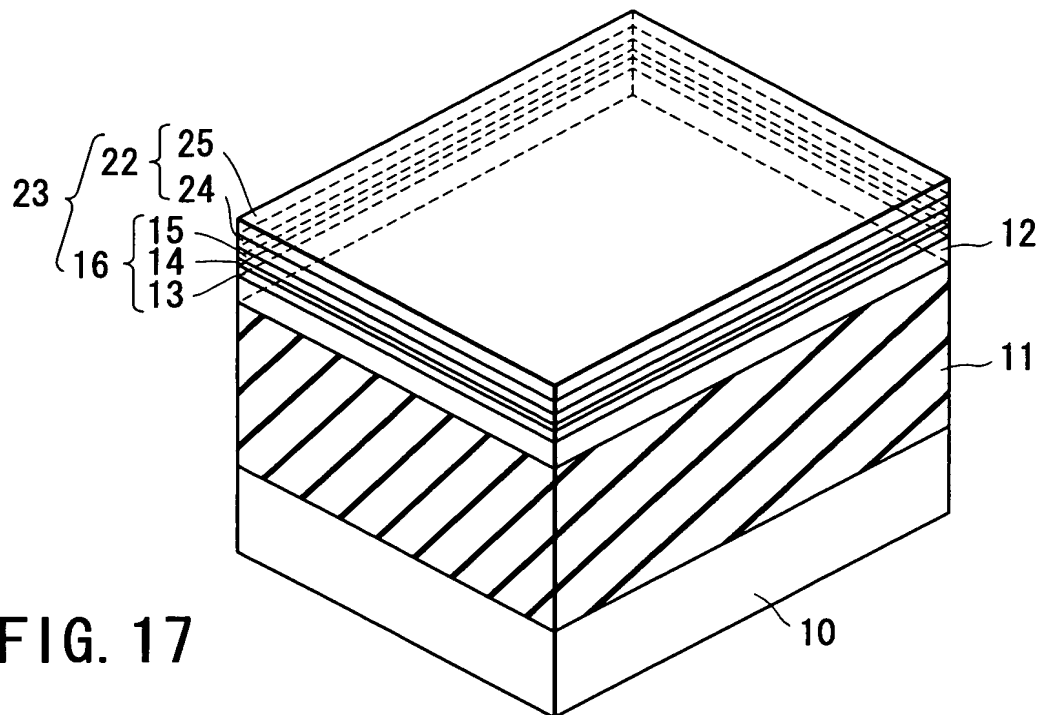


FIG. 17

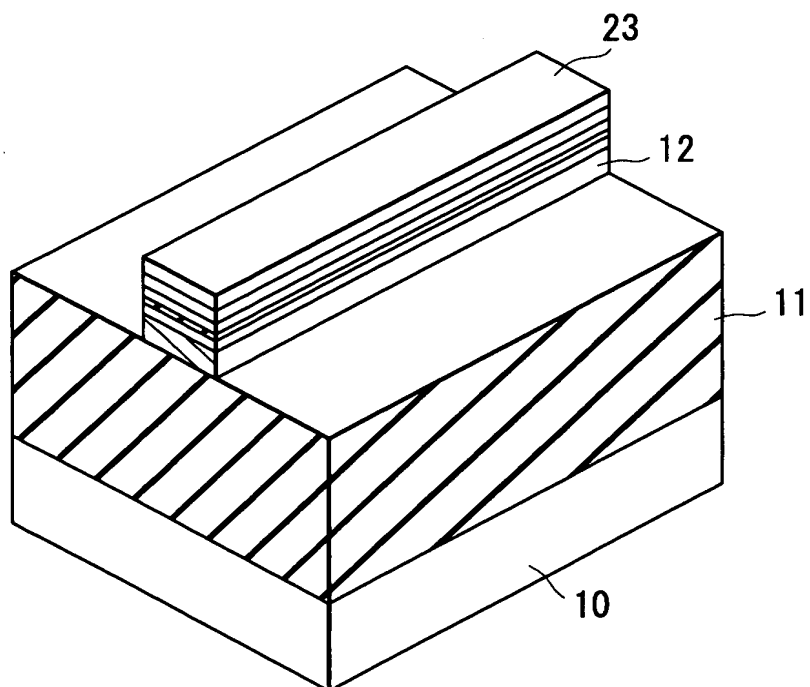


FIG. 18

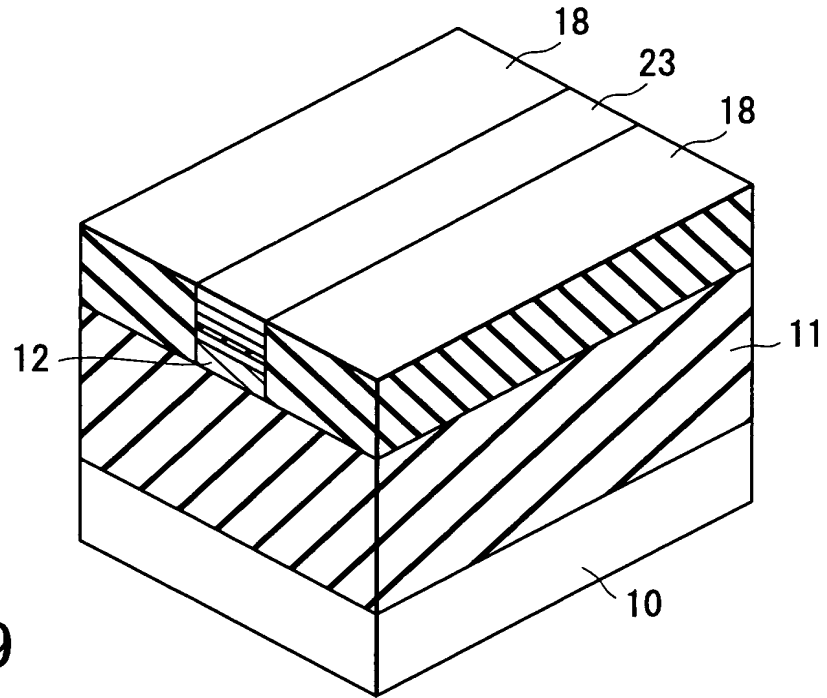


FIG. 19

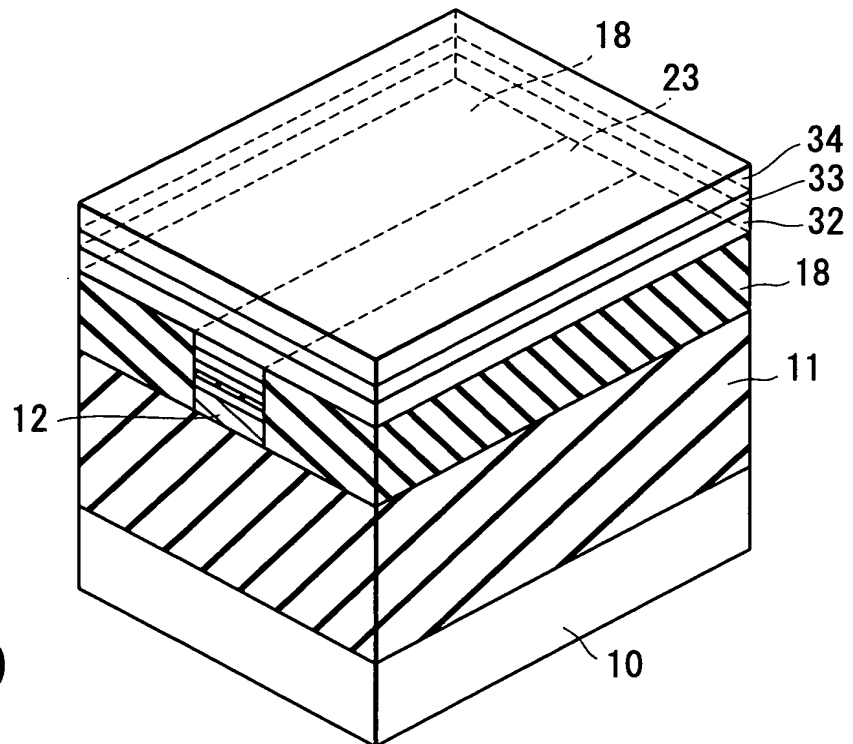


FIG. 20

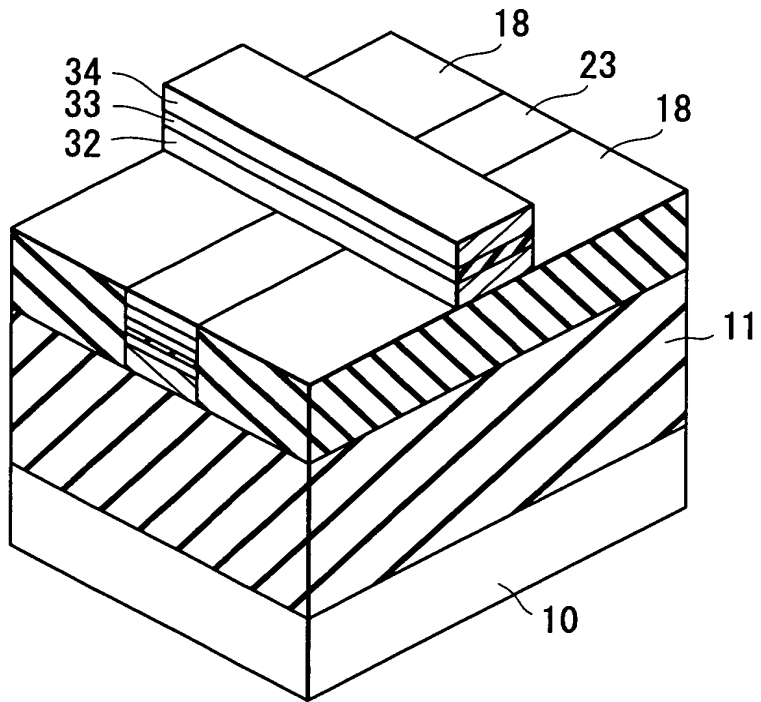


FIG. 21

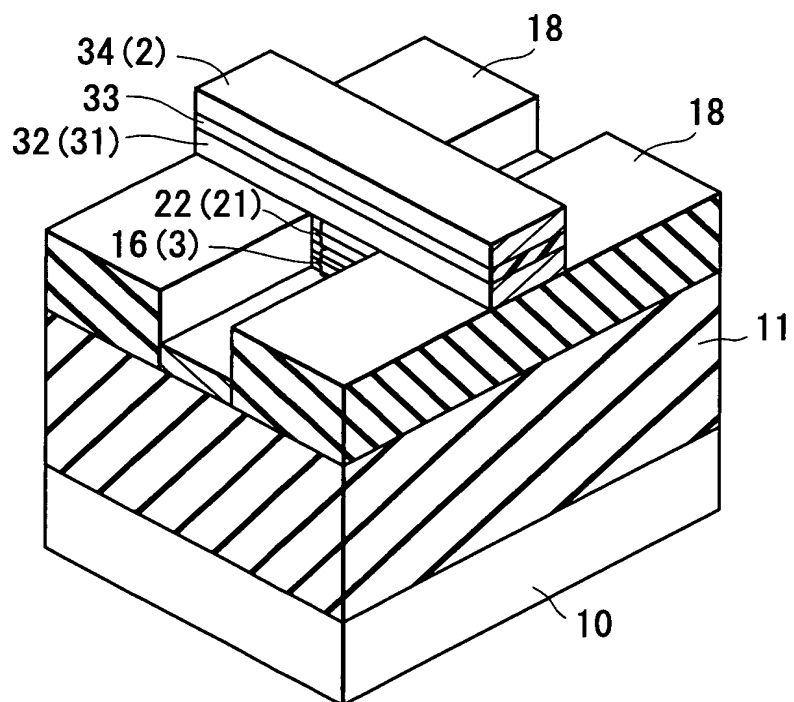
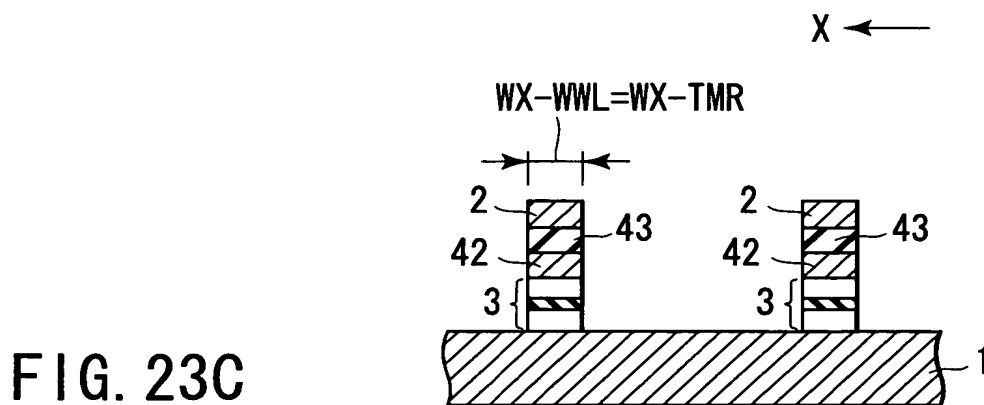
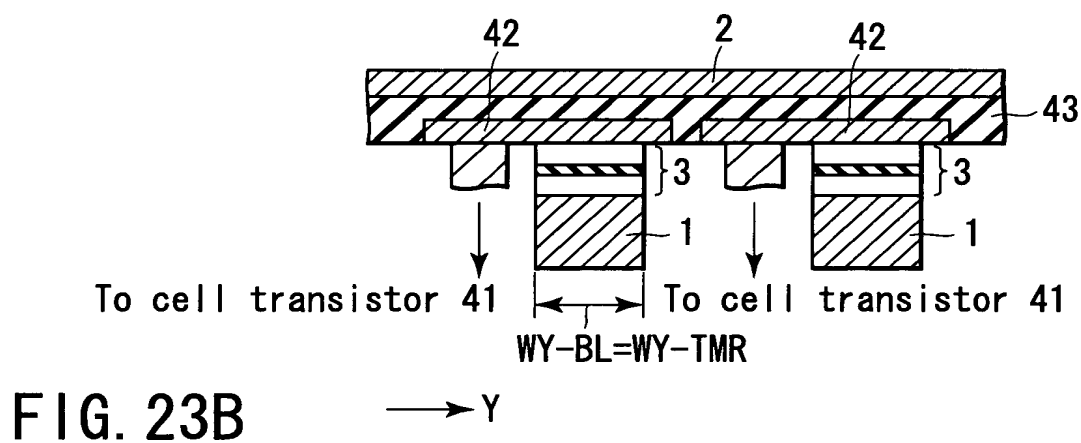
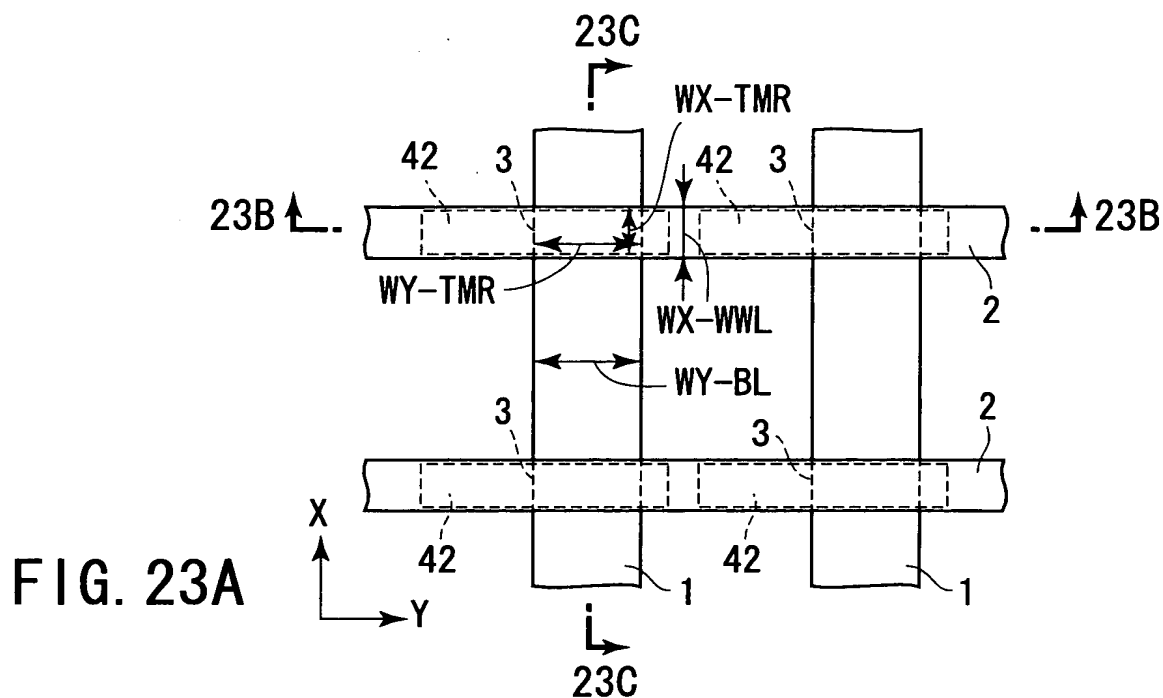


FIG. 22



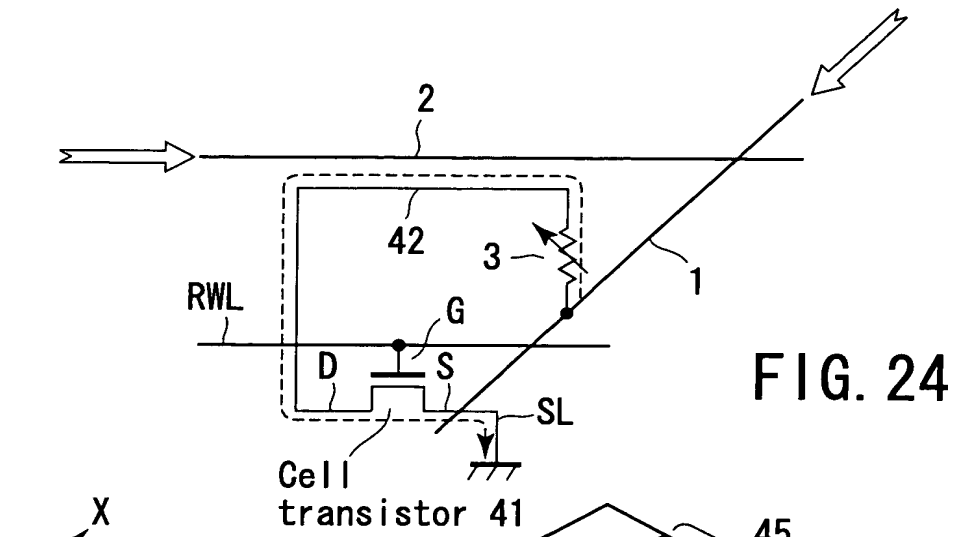


FIG. 24

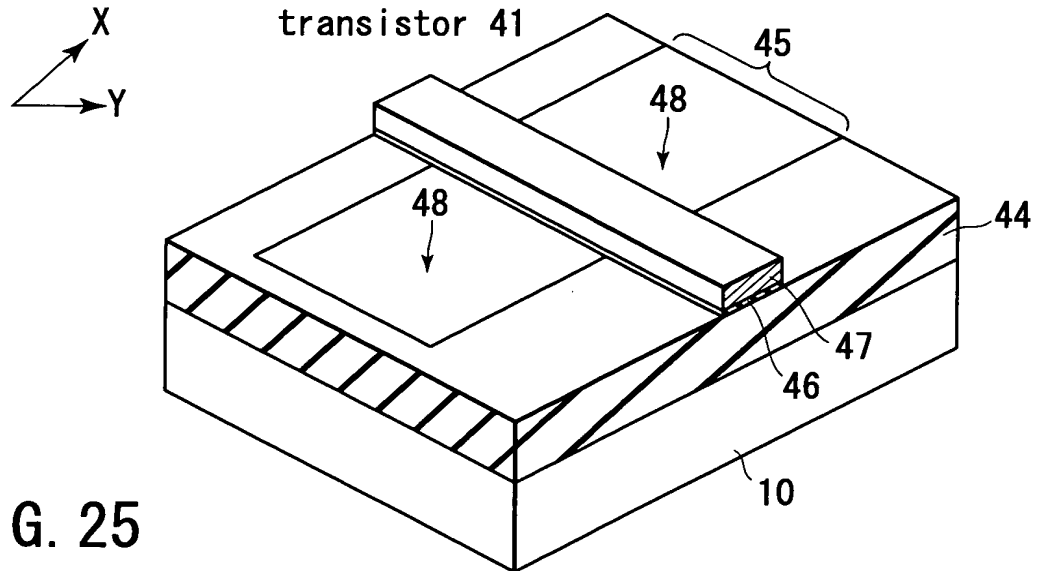


FIG. 25

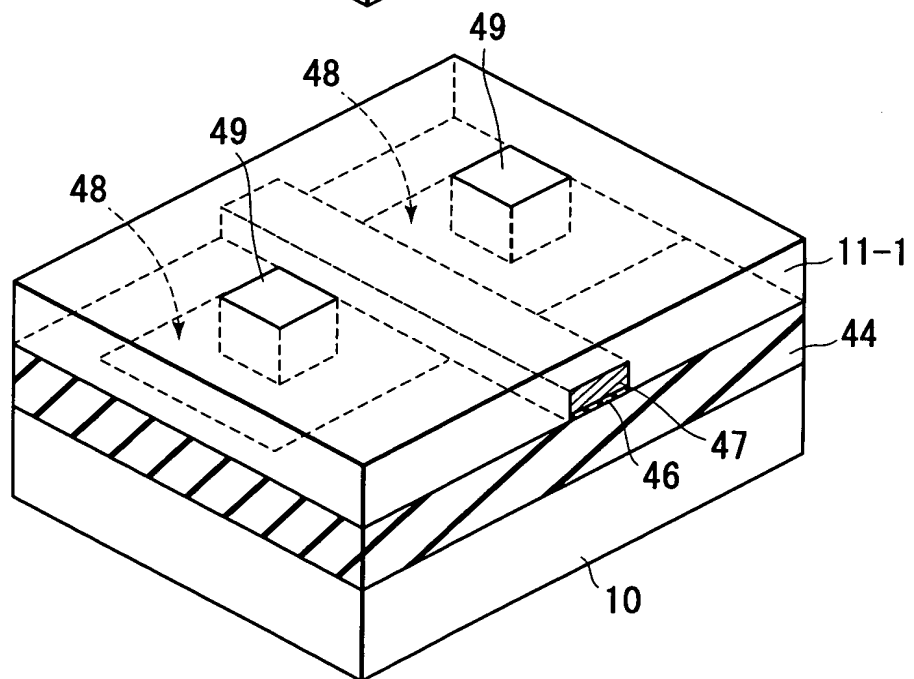


FIG. 26

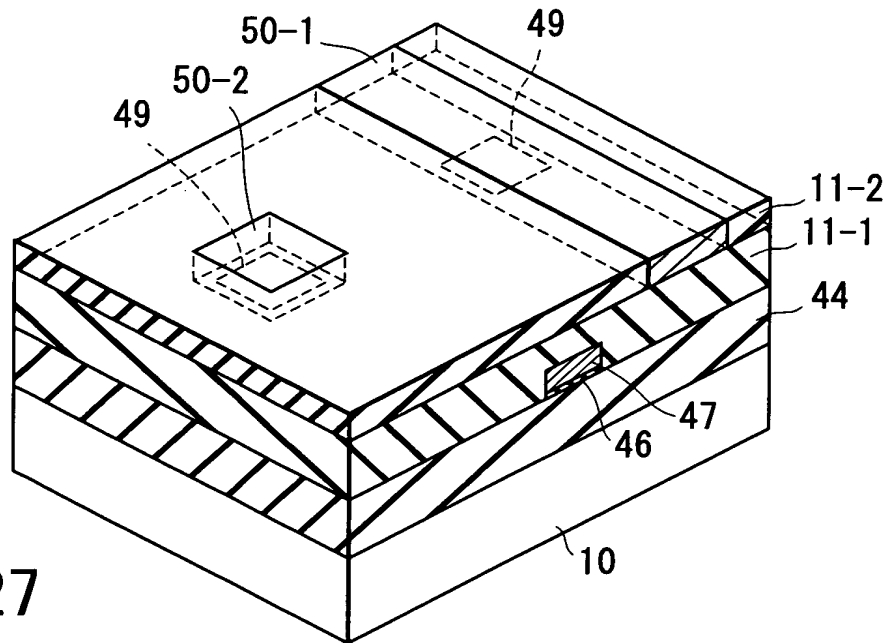


FIG. 27

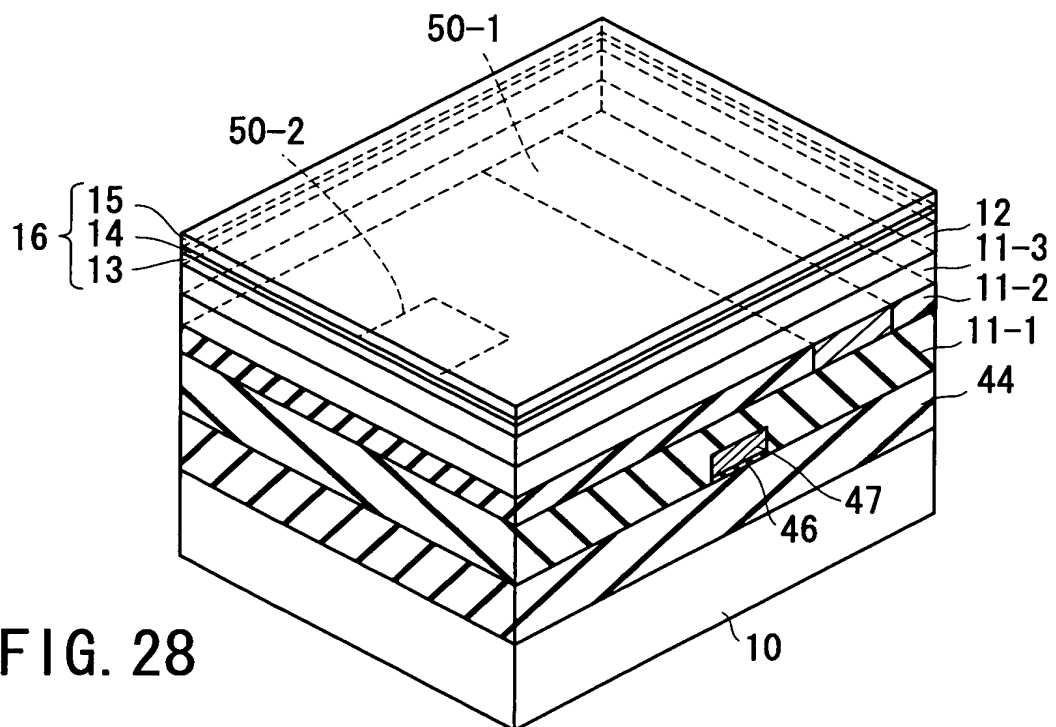


FIG. 28



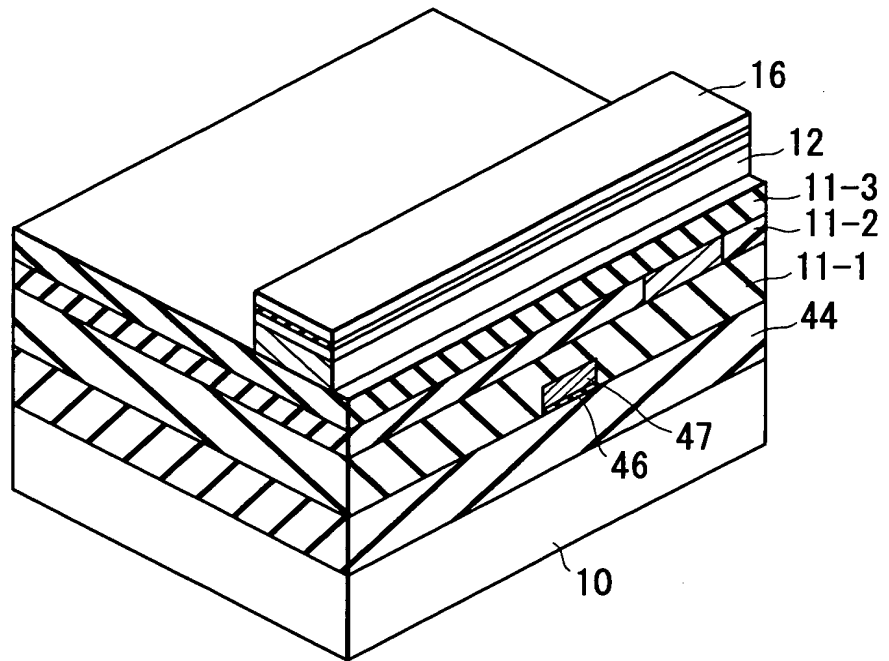


FIG. 29

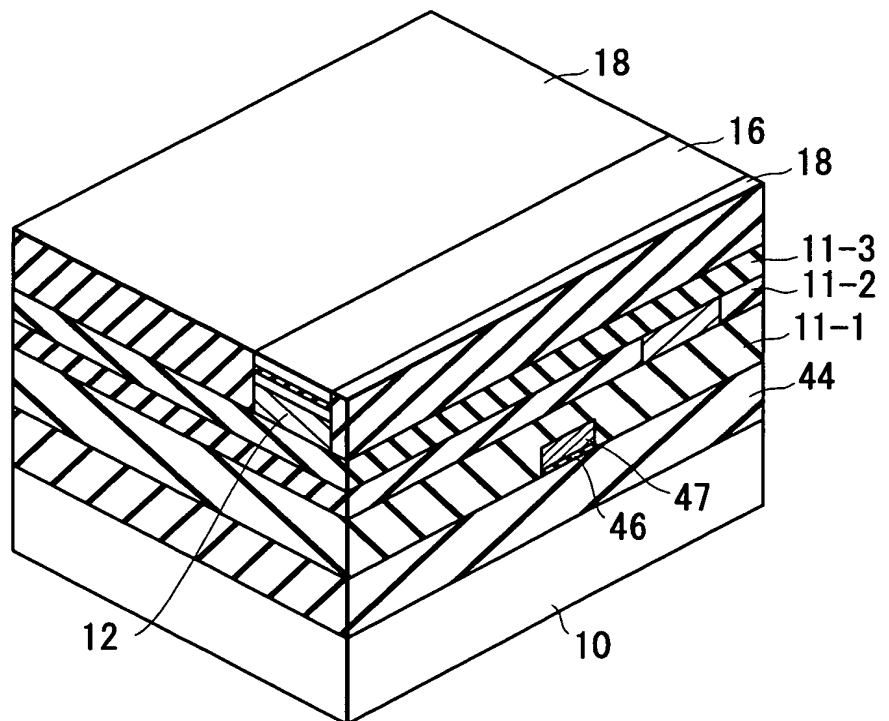


FIG. 30

FIG. 31

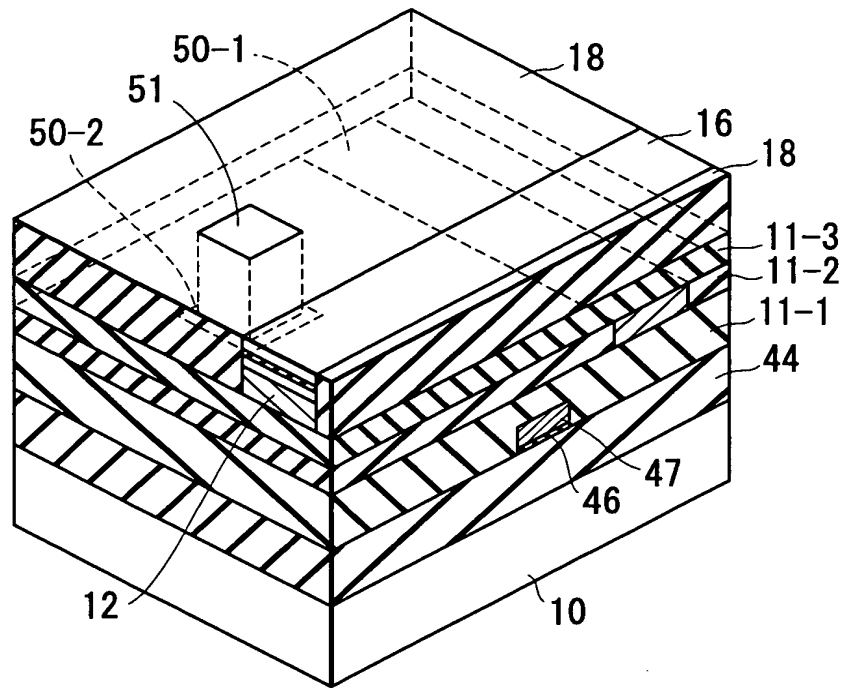
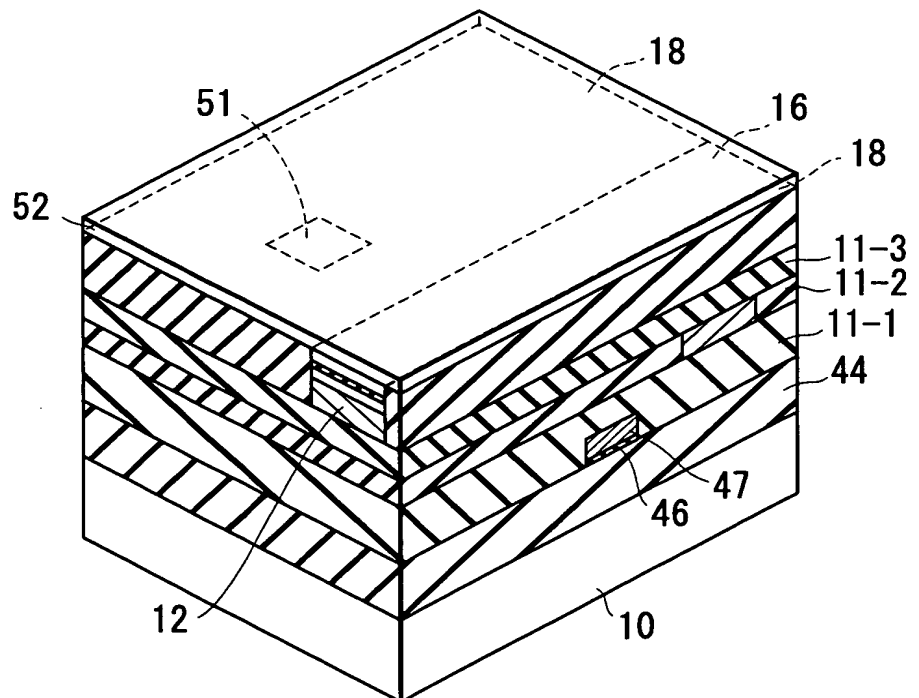
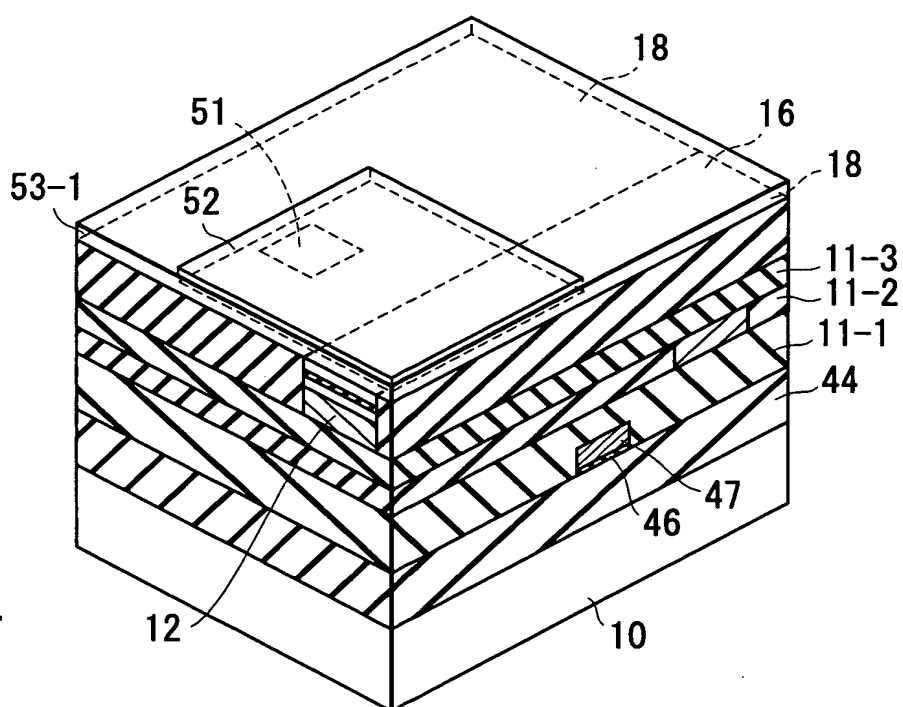
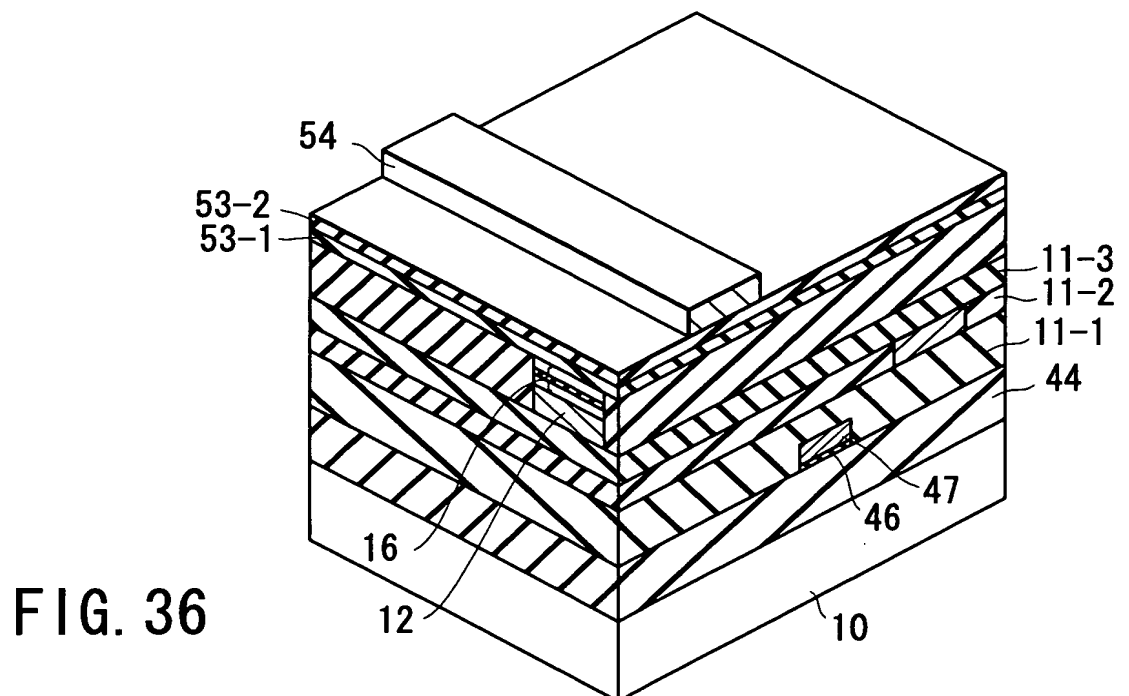
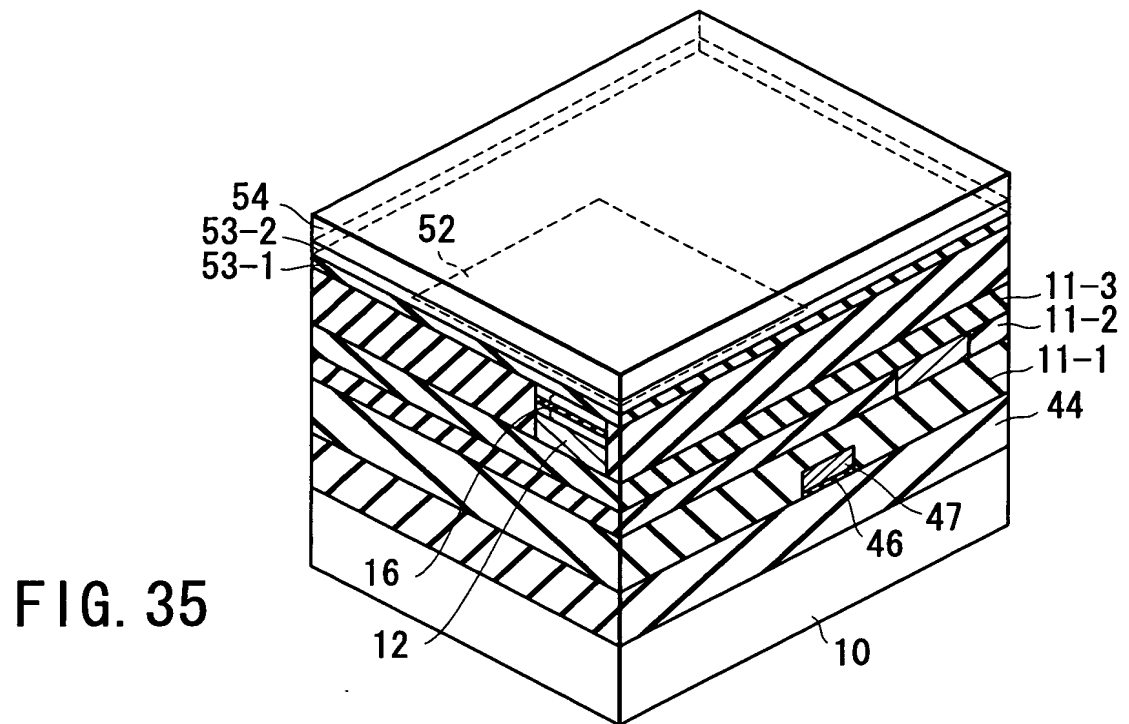


FIG. 32







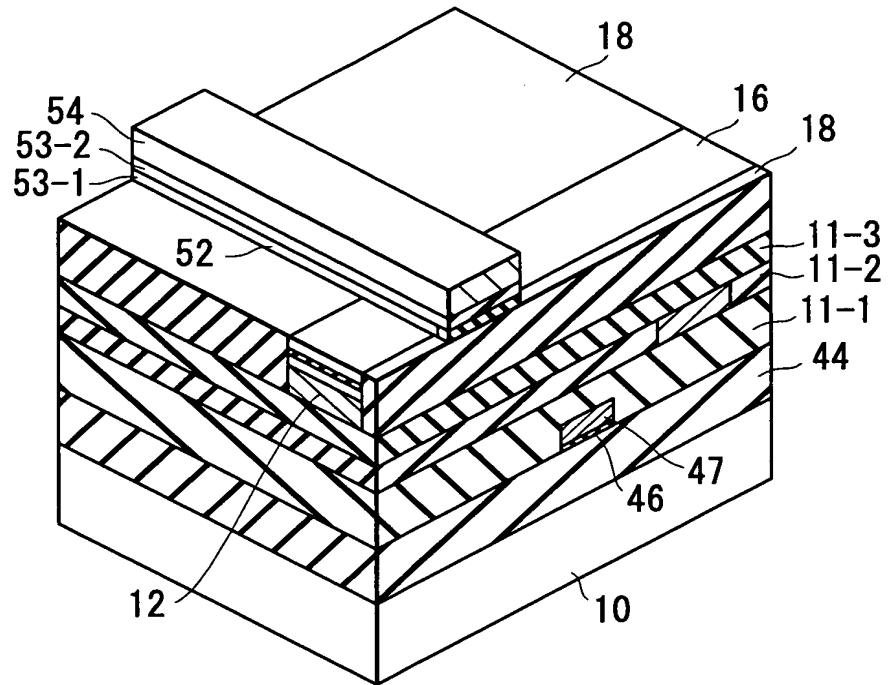


FIG. 37

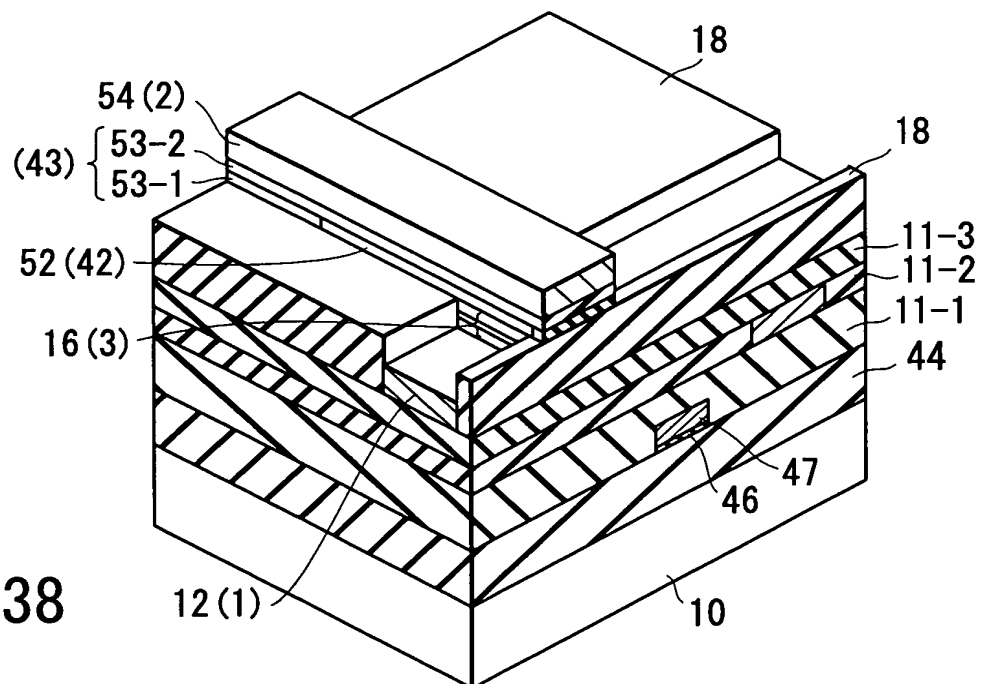
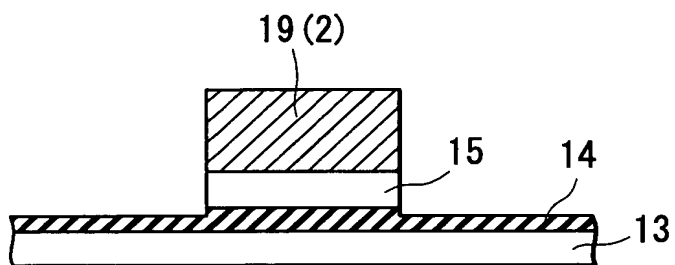
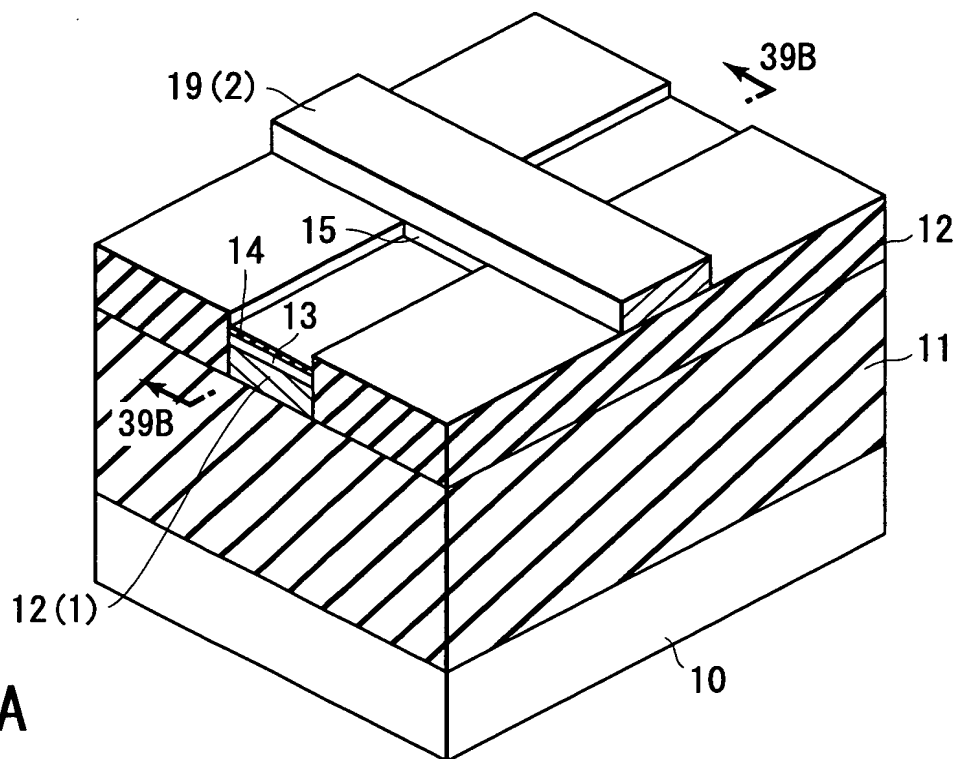


FIG. 38



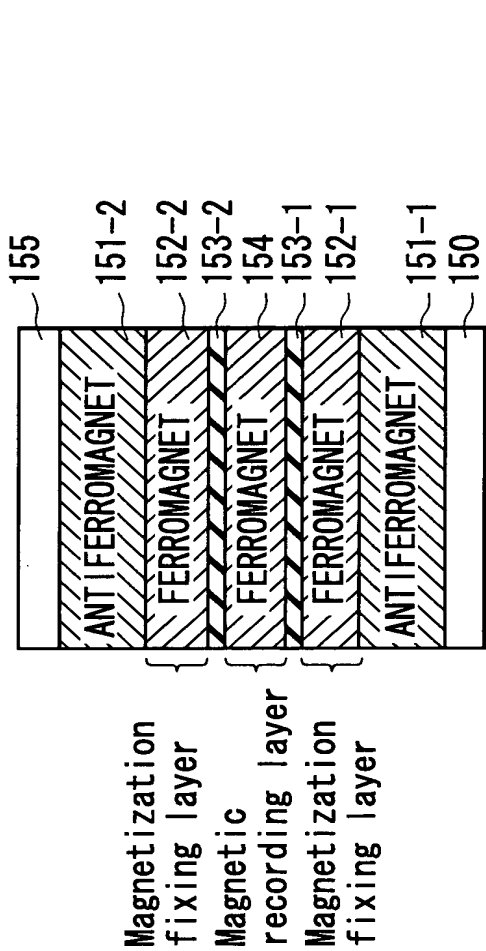


FIG. 40B

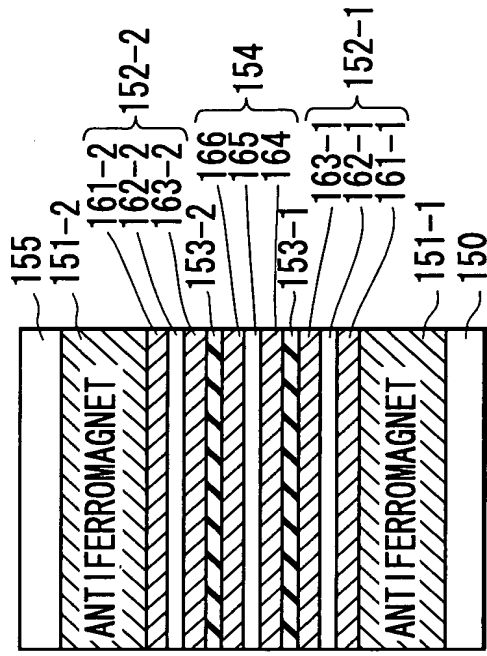


FIG. 40D

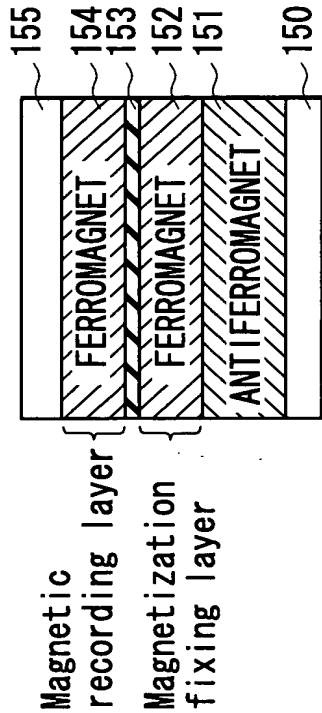


FIG. 40A

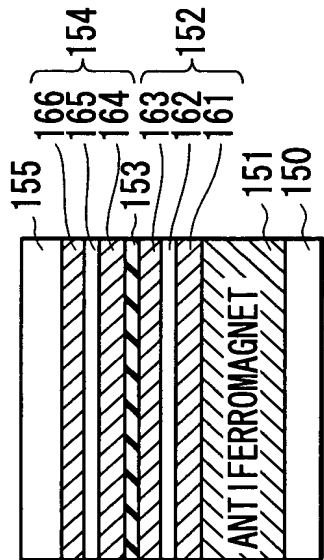


FIG. 40C

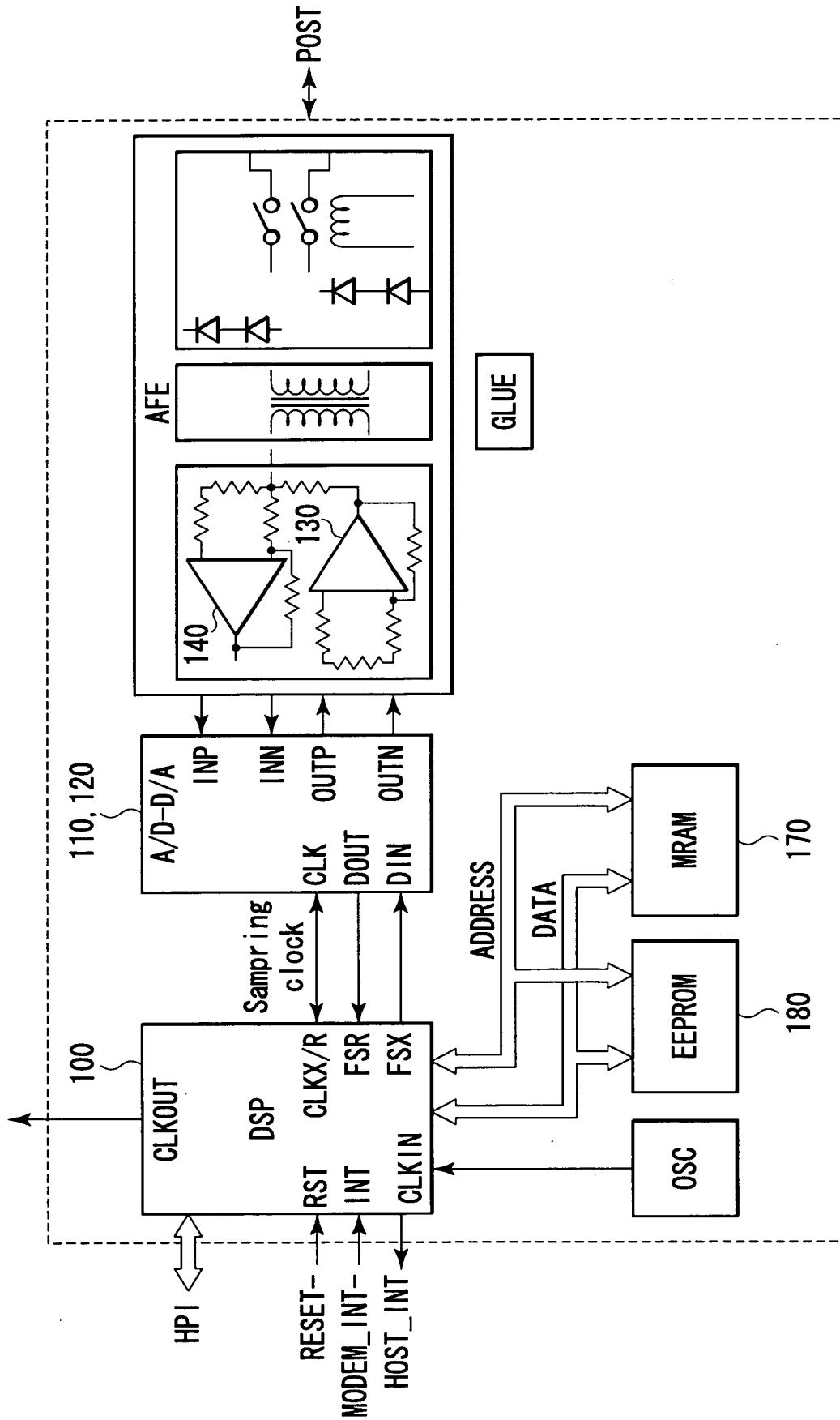


FIG. 41



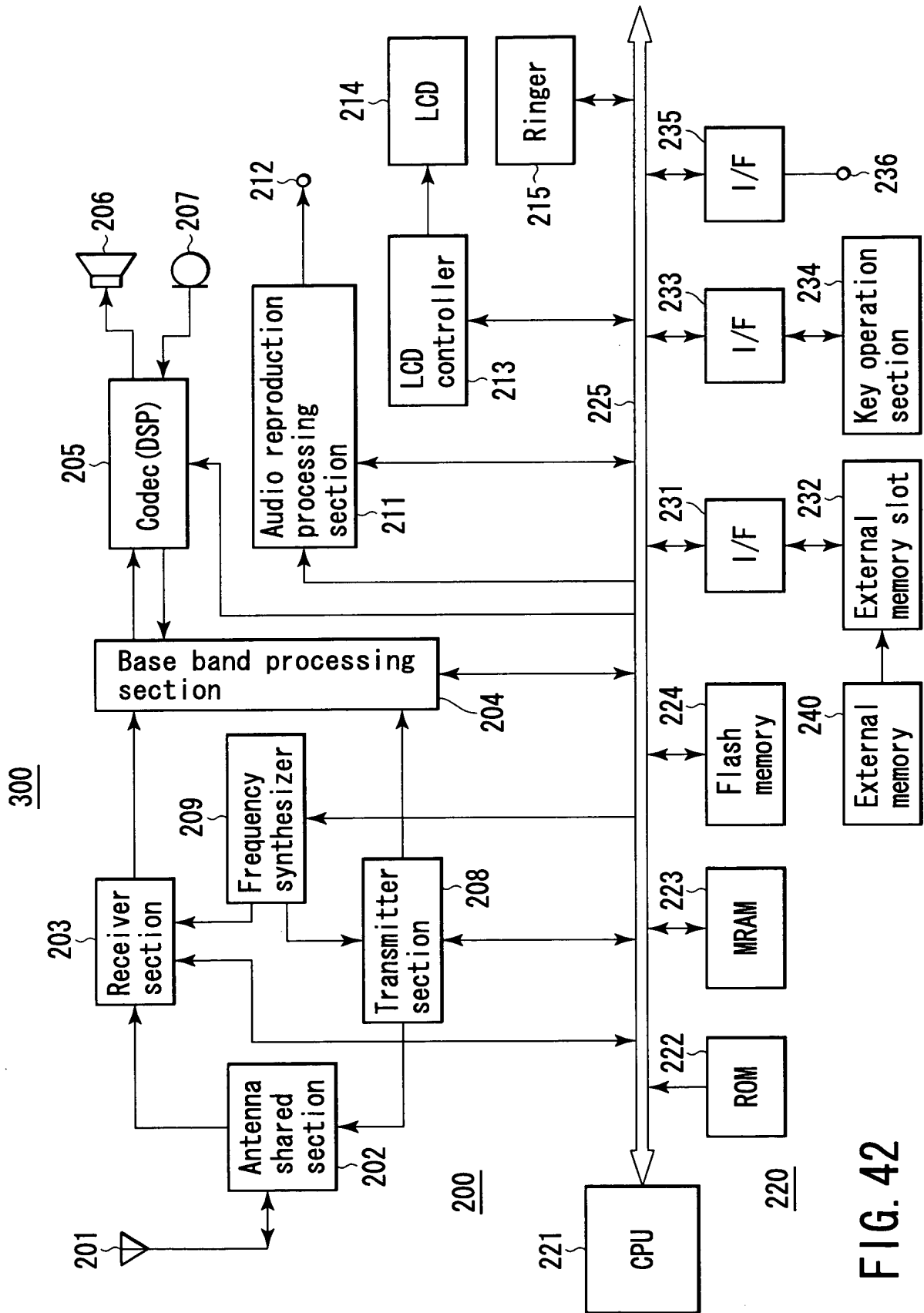


FIG. 42

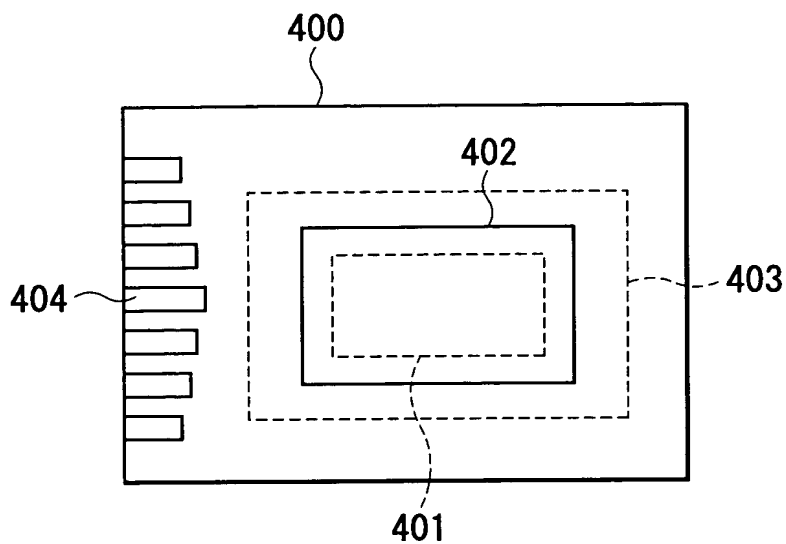
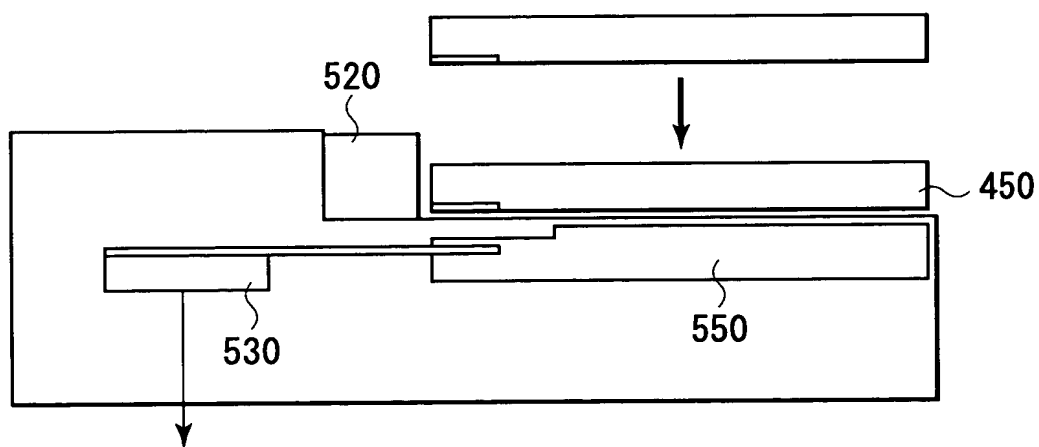
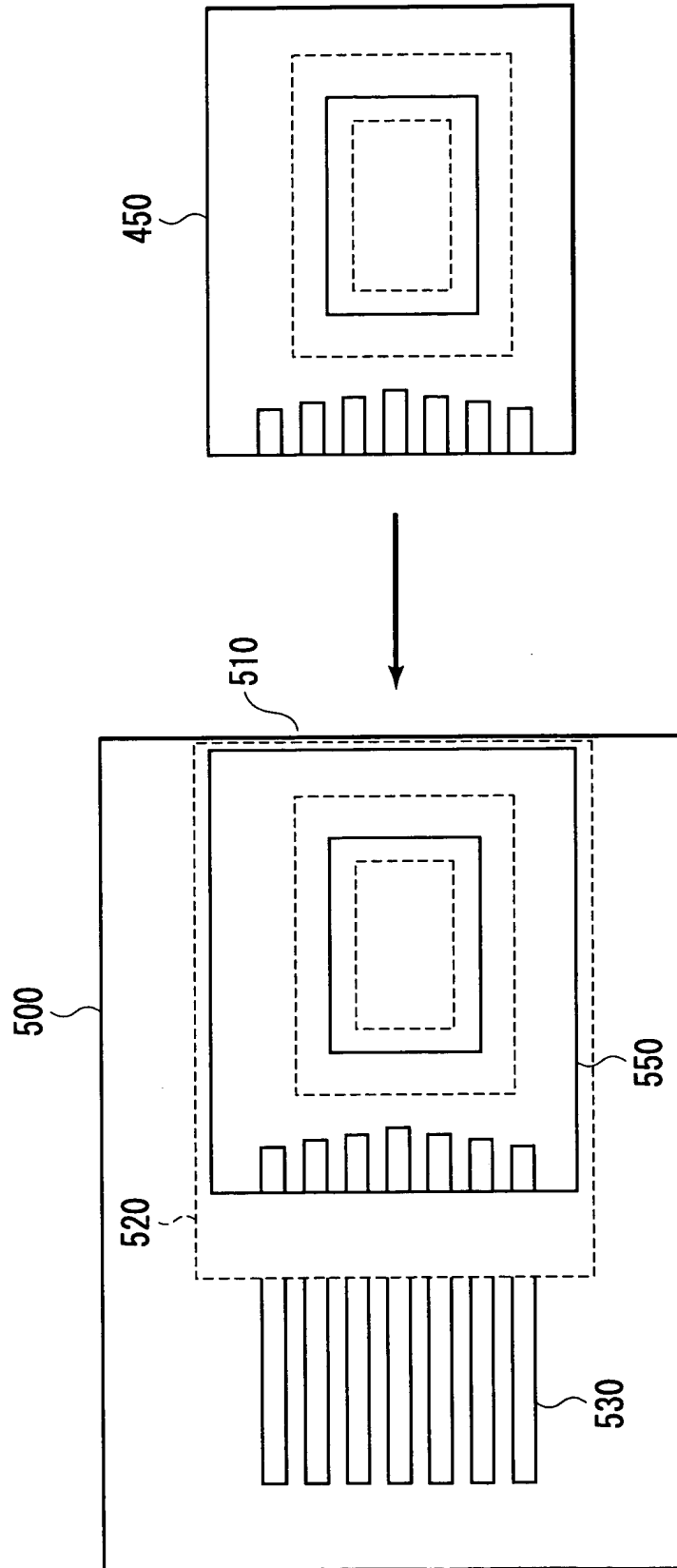


FIG. 43



Transfer first MRAM data to  
write control section

FIG. 46



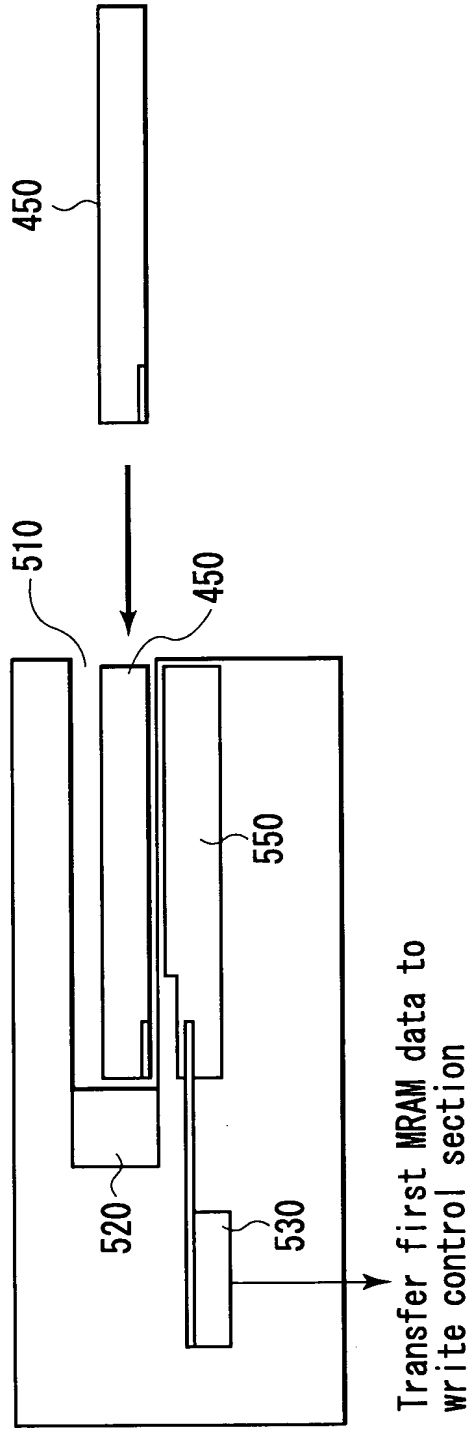


FIG. 45

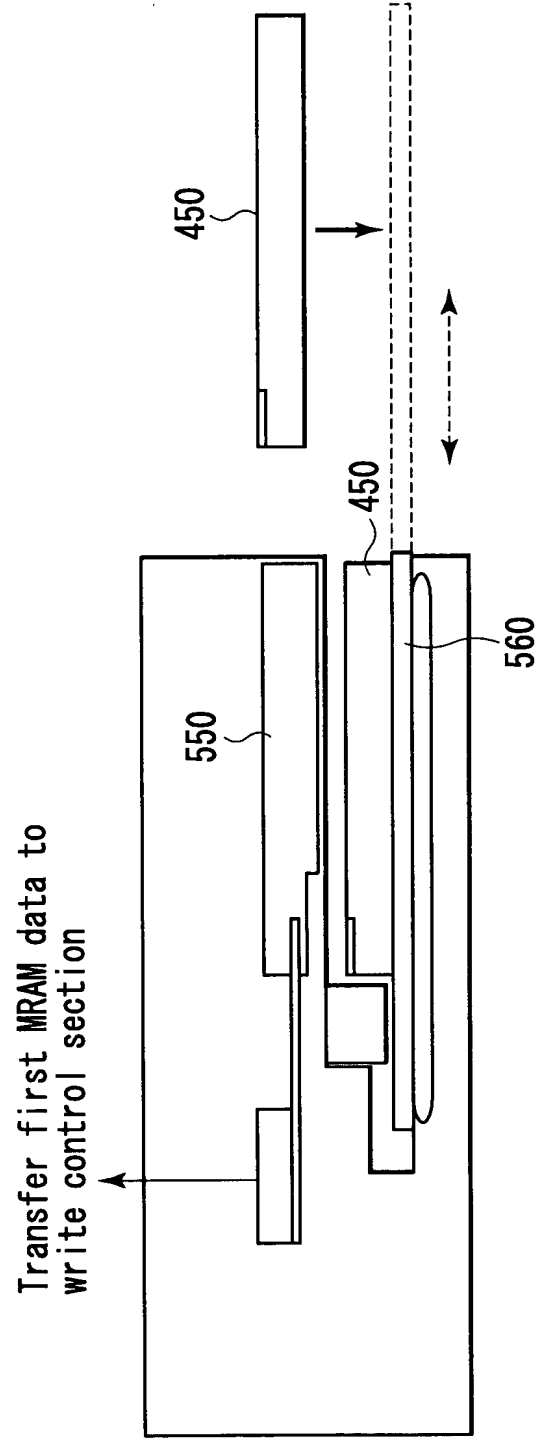


FIG. 47

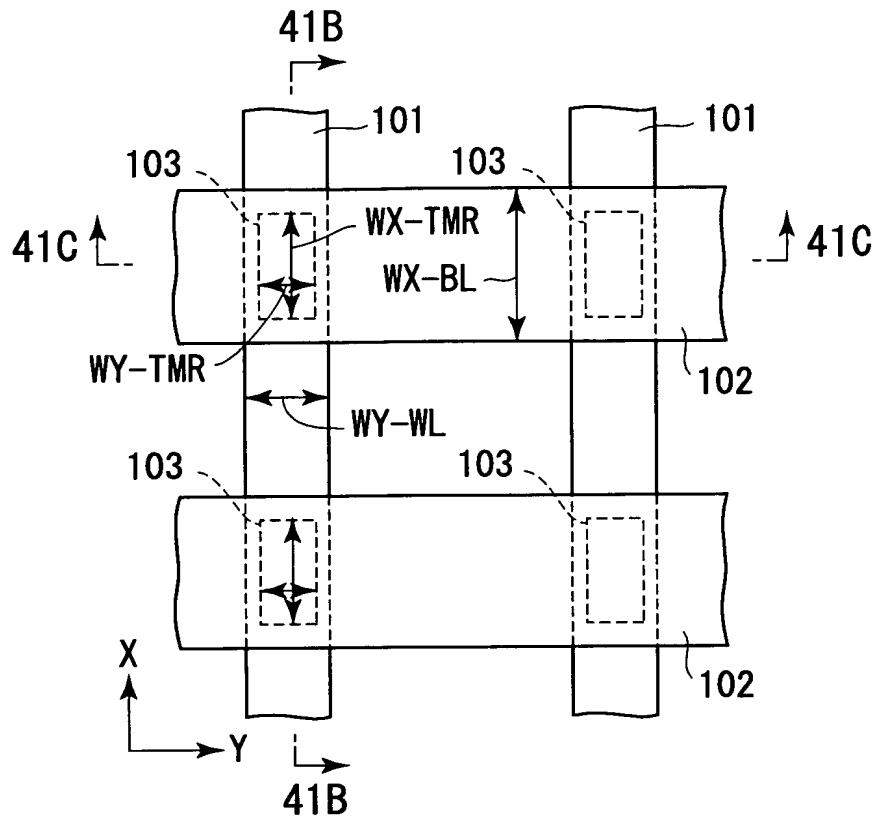


FIG. 48A

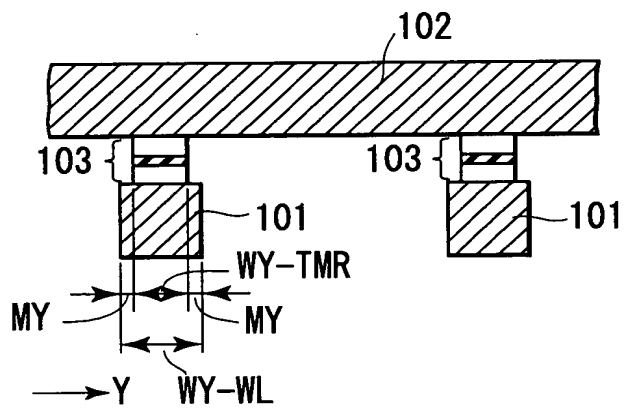


FIG. 48B

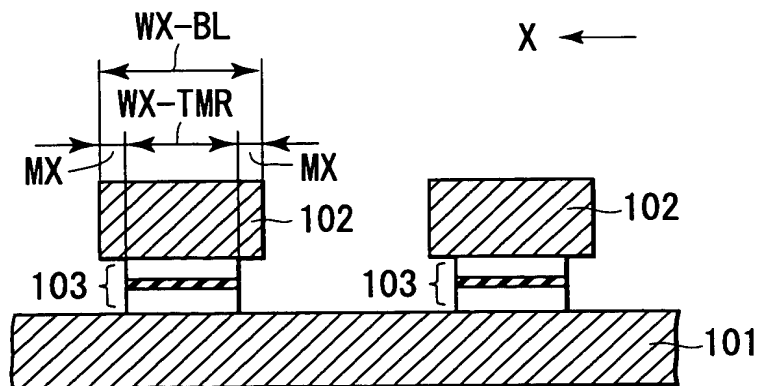


FIG. 48C

Ideal MTJ shape

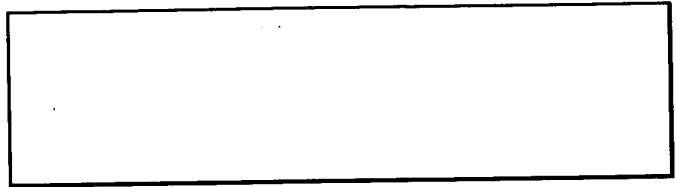


FIG. 49A

Ideal MTJ shape

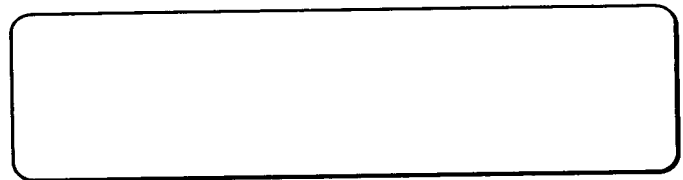


FIG. 49B

Actual MTJ shape

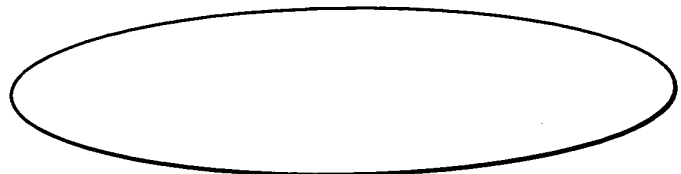


FIG. 49C